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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,847	05/25/2001	Stefanos Kaxiras	Diodato 9-7-17-2	5066
7590	07/26/2004		EXAMINER	
Ryan, Mason & Lewis, LLP 1300 Post Road, Suite 205 Fairfield, CT 06430			CAO, CHUN	
			ART UNIT	PAPER NUMBER
			2115	

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

WEN

Office Action Summary	Application No.	Applicant(s)
	09/865,847	KAXIRAS ET AL.
	Examiner	Art Unit
	Chun Cao	2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 25 May 2001.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-5,9-17,20,21,23-29 and 31-35 is/are rejected.
- 7) Claim(s) 6-8,18,19,22 and 30 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>4/16/04, 5/31/02</u> | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. Claims 1-35 are presented for examination.
2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

Claim Rejections - 35 USC § 101

Double Patenting

3. Claims 1-26 are provisionally rejected under the judicially created doctrine of double patenting over claims 1-28 of copending Application No. 10/060661. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: removes power said associated cache line after a decay interval.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 U.S.C. § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-5, 9-14, 17, 20, 21, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherlock et al. (Sherlock), US patent no. 6,157,977 in view of Fuller (Fuller), U.S. Patent No. 5,632,038.

As per claim 1, Sherlock discloses a cache memory [fig. 2], comprising:
a plurality of cache lines for storing a value from main memory [col. 5, lines 3-6;
col. 8, lines 8-10]; and
a timer [CLA 58, col. 4, lines 66-67] associated with each of said plurality of cache lines [col. 5, lines 19-20].

Sherlock does not explicitly teach of using the timer configured to control signal that removes power to said associated cache line after a decay interval.

Fuller teaches of using the timer configured to control signal that removes power said associated cache line after a decay interval [col. 3, lines 18-22; col. 6, lines 30-32; col. 7, lines 25-38; col. 7, line 64-col. 8, line 2].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Sherlock and Fuller because the specific teachings of Fuller stated above would improve the efficiency of power consumption Sherlock's system by using a timer to monitor the activities of the cache lines.

As per claim 2, Sherlock discloses a timer associated with a given cache line is reset each time said associated cache line is accessed [col. 5, lines 11-13; col. 8, lines 14-15].

As per claim 3, Fuller discloses that decay interval is variable [periods of inactivity, col. 3, lines 19-20].

As to claims 4 and 5, inherently, Fuller teaches that variable decay interval can be increased to increase performance and lowered to save power [col. 3, lines 23-28].

As per claim 9, Sherlock discloses that a timer is a k bit timer and said timer receives a tick from any source [col. 4, lines 58, 66-67].

As per claim 10, Sherlock discloses that timer is any k-state finite state machine (FSM) that can function logically as a counter [fig. 3, col. 4, lines 58, 66-67].

As per claim 11, Fuller discloses a dirty bit associated with each of said cache lines to indicate when a contents of said cache line must be written back to main memory before said power is removed from said associated cache line after said decay interval [col. 7, lines 28-38].

As per claim 12, Sherlock discloses that one or more of said timer associated with plurality of cache lines are cascaded to distribute said writing back to main memory [fig. 3].

As to claims 13 and 14, Fuller discloses of removing power from said associated cache line resets a valid field associated with said cache line and a signal is configured to remove a potential from said cache line [col. 3, lines 18-22; col. 6, lines 30-32; col. 7, lines 25-38; col. 7, line 64-col. 8, line 2].

As per claim 17, Sherlock discloses a timer is an analog device [CLA 58, fig. 3].

As to claims 20, 21, 23, 24, Sherlock and Fuller together teach the claimed system. Therefore Sherlock and Fuller together teach the claimed method of steps to carry out the system.

6. Claims 15, 16, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherlock et al. (Sherlock), US patent no. 6,157,977 in view of Fuller (Fuller), U.S. Patent No. 5,632,038 and Takahashi (Takahashi), US patent no. 6,345,336.

As to claims 15 and 25, Sherlock and Fuller both do not teach a first access to a cache line that has been powered down results in a cache miss, resets said corresponding timer and restores power to said cache line.

Takahashi teaches a first access to a cache line that has been powered down results in a cache miss, resets said corresponding timer and restores power to said cache line [col. 5, lines 36-48].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Sherlock and Fuller and Takahashi because the specific teachings of Takahashi stated above would further improve the reliability Sherlock's system by restoring power to the cache lines.

As to claims 16 and 26, Fuller inherently teaches of a first access to a cache line that has been powered down is delayed by a period of time that permits said cache line to stabilize after power is restored [col. 5, lines 36-48].

7. Claims 27-29 and 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherlock et al. (Sherlock), US patent no. 6,157,977 in view of Stein et al. (Stein), Session V: "Storage Array and Sense/Refresh Circuit for Single-Transistor Memory Cells" 1972, pages 56-57 and Fuller (Fuller), U.S. Patent No. 5,632,038.

As to claims 27 and 28, Sherlock discloses a plurality of cache lines for storing a value from main memory [col. 5, lines 3-6; col. 8, lines 8-10]; and each of said cache lines comprised of one or more random access memory (RAM) cells and each of said RAM cells being refreshed each time said cache line is accessed [col. 5, lines 11-13; col. 8, lines 14-15], and a timer associated with each of said plurality of cache lines, each of said timers controlling a signal that resets a valid bit associated with said cache line after said safe period a timer [CLA 58, col. 4, lines 66-67; col. 5, lines 11-13; col. 8, lines 14-15].

Sherlock does not explicitly teach of comprising of one or more dynamic random access memory (DRAM) cells.

Stein discloses one or more dynamic random access memory (DRAM) cells [page 56, left column, paragraphs 1-2].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Sherlock and Stein because the specific teachings of Stein stated above would improve the functionality Sherlock's system by using a DRAM cells to utility the system.

As per claim 29, Stein discloses that DRAM cells are embodied as 4-T DRAM cells [page 56, left column, paragraph 1].

As per claim 31, Sherlock discloses that a timer is a k bit timer and said timer receives a tick from any source [col. 4, lines 58, 66-67].

As per claim 32, Sherlock discloses that timer is any k-state finite state machine (FSM) that can function logically as a counter [fig. 3, col. 4, lines 58, 66-67].

As per claim 33, Fuller discloses a dirty bit associated with each of said cache lines to indicate when a contents of said cache line must be written back to main memory before said power is removed from said associated cache line after said decay interval [col. 7, lines 28-38].

As to claims 34 and 35, Sherlock and Stein together teach the claimed system. Therefore Sherlock and Stein together teach the claimed method of steps to carry out the system.

Allowable Subject Matter

8. Claims 6-8, 18, 19, 22 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"Automatic Cache Line Access Monitoring" IBM TDB, Vol. 37, No. 6A, June 1994, page 299, teaches of turning off cache line after the data is accessed by the program.

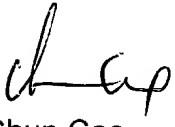
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 703-308-6106. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 306-5631.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Chun Cao

July 22, 2004